What is claimed is:

1. A non-volatile memory comprising:

an array of non-volatile memory cells arranged in columns using bit lines; and

a verify circuit selectively coupled to the bit lines to determine if the memory cells have a erase level that is within a erase level window defined by first and second reference signals.

2. The non-volatile memory of claim 1 further comprises a current-to-voltage converter coupled between a selected one of the bit lines and the verify circuit.

3. The non-volatile memory of claim 1 wherein the verify circuit comprises:

a first comparator with a reference input coupled to receive the first reference signal, and a second input coupled to the selected one of the bit lines; and

a second comparator with a reference input coupled to receive the second reference signal and a second input is coupled to the selected one of the bit lines.

4. The non-volatile memory of claim 3 further comprises:

first and second reference currents circuits; and

first and second current-to-voltage converters coupled respectively between the first and second reference current circuits and the first and second comparators, wherein the first and second current-to-voltage converters respectfully provide the first and second reference voltages.

5. The non-volatile memory of claim 3 further comprises a reference current circuit and a current-to-voltage converter coupled respectively between the reference current circuit and the first and second comparators, wherein the current-to-voltage converter provides the first and second reference signals.

6. The non-volatile memory of claim 1 wherein the memory cells comprise a plurality of floating gate memory cells.

7. A bit line verify system comprising:

a first comparator to compare a bit line current with a first reference current and produce a first output signal;

a second comparator to compare the bit line current with a second reference current and produce a second output signal; and

control circuitry to perform erase operations in response to the first and second output signals.

8. The bit line verify system of claim 7 further comprises first and second reference current circuits to respectfully provide the first and second reference currents.

9. The bit line verify system of claim 7 further comprises first and second current sources to respectively provide the first and second reference current.

10. The bit line verify system of claim 9 wherein the first current source comprises a floating gate transistor programmed to conduct a specific amount of current in response to a control signal.

11. The bit line verify system of claim 7 wherein the memory cells comprise a plurality of floating gate memory cells.

12. A memory device with an erase verify system comprising:

a memory array having a plurality of memory cells coupled to a bit line;

a first comparator to compare a bit line voltage with a first reference voltage and produce a first output signal;

a second comparator to compare the bit line voltage with a second reference voltage and produce a second output signal; and

control circuitry to perform erase operations in response to the first and second output signals.

13. The memory device of claim 12 further comprises a current-to-voltage converter coupled between the bit line and the first and second comparators.

14. The memory device of claim 13 wherein the current-to-voltage converter comprises:

a resistor; and

an activation circuit to selectively allow a current to flow through the resistor, wherein the activation circuit is coupled between the resistor and the bit line.

15. The memory device of claim 14 wherein the activation circuit comprises:

an activation transistor having a source coupled to the resistor; and

an inverter circuit coupled between a gate of the activation transistor and a drain of the activation transistor, wherein the drain of the activation transistor is coupled to the bit line.

16. The memory device of claim 12 further comprises:

first and second reference current circuits; and

first and second current-to-voltage converters coupled respectively between the first and second reference current circuits and the first and second comparators, wherein the first and second current-to-voltage converters respectfully provide the first and second reference voltages.

17. The memory device of claim 16 wherein the first and second current-to-voltage converter each comprise:

a resistor; and

an activation circuit to selectively allow a current to flow through the resistor, wherein the activation circuit is coupled between the resistor and either the first or second reference current circuit.

18. The memory device of claim 17 wherein the activation circuit comprises:

an activation transistor having a source coupled to the resistor; and

an inverter circuit coupled between a gate of the activation transistor and a drain of the activation transistor, wherein the drain of the activation transistor is further coupled to either the first or second reference current circuit.

19. The memory device of claim 12 further comprising:

a reference current circuit; and

a current-to-voltage converter coupled between the reference current circuit and the first and second comparators, wherein the current-to-voltage converter provides the first and second reference voltages.

20. The memory device of claim 19 wherein the current-to-voltage converter comprises:

a first resistor;

a second resistor coupled in series with the first resistor; and

an activation circuit to selectively allow a current to flow through the first and second resistors, wherein the activation circuit is coupled between the second resistor and the reference current circuit.

21. The memory device of claim 20 wherein the activation circuit comprises:

an activation transistor having a source coupled to the second resistor; and

an inverter circuit coupled between a gate of the activation transistor and a drain of the activation transistor, the drain of the activation transistor is coupled to the reference current circuit.

22. The memory device of claim 12 further comprising:

first and second control current sources; and

first and second current-to-voltage converters coupled respectively between the first and second control current sources and the first and second comparators, wherein the first and second current-to-voltage converters respectfully provide the first and second reference voltages.

23. The memory device of claim 22 wherein the first and second control current sources each comprise a floating gate transistor programmed to conduct a specific amount of current in response to a control signal.

24. The memory device of claim 12 further comprises:

a control current source; and

a current-to-voltage converter coupled respectively between the reference current source and the first and second comparators, wherein the current-to-voltage converter provides first and second reference voltage.

25. The memory device of claim 24 wherein the control current source comprises a floating gate transistor programmed to conduct a specific amount of current in response to a control signal.

26. The memory device of claim 12 wherein the plurality of memory cells comprise a plurality of floating gate memory cells.

27. A memory system comprising:

an external processor; and

a non-volatile memory coupled to the external processor, the non-volatile memory comprises,

an array of memory cells arranged in columns coupled to bit lines,

a first comparator to compare a bit line voltage with a first reference voltage and produce a first output signal,

a second comparator to compare a bit line voltage with a second reference voltage and produce a second output signal,

a current-to-voltage converter coupled between the bit lines and the first and second comparators,

first and second reference current circuits,

first and second current-to-voltage converters coupled respectively between the first and second reference current circuits and the first and second comparators, wherein the first and second current-to-voltage converters respectfully provides the first and second reference voltages, and

a control circuit coupled to receive the first and second output signals and perform erase operations in response thereto.

28. A memory system comprising:

an external processor; and

a non-volatile memory coupled to the external processor, the non-volatile memory comprises,

an array of memory cells arranged in columns coupled to bit lines,

a first comparator to compare a bit line current with a first reference current and produce a first output signal,

a second comparator to compare a bit line current with a second reference current and produce a second output signal,

first and second reference current circuits to provide first and second reference currents, and

a control circuit coupled to receive the first and second output signals and perform erase operations in response thereto.

29. A method of erase verifying a non-volatile memory cell comprising:

generating a first reference current;

generating a second reference current; and

comparing a bit line current from a column coupled to the non-volatile memory cell with the first reference current and the second reference current.

30. A method of erase verifying a non-volatile memory cell comprising:

generating a first reference voltage;

generating a second reference voltage; and

comparing a bit line voltage from a column coupled to the non-volatile memory cell with the first reference voltage and the second reference voltage.

31. A method of ease verifying a non-volatile memory cell comprising:

providing a first reference current;

converting the first reference current to a first reference voltage;

providing a second reference current;

converting the second reference current to a second reference voltage;

converting a current from a bit line coupled to the memory cell to a bit line voltage;

comparing the bit line voltage with the first reference voltage and the second reference voltage; and

identifying if the memory cell is over-erased, under-erased or erased.

32. A method of erase verifying a non-volatile memory cell comprising:

providing a reference current;

converting the reference current to a first reference voltage and a second reference voltage;

converting a current from a bit line coupled to the memory cell to a bit line voltage;

comparing the bit line voltage with the first reference voltage and the second reference voltage; and

identifying if the memory cell is over-erased, under-erased or erased.

33. A method of erase verifying a non-volatile memory cell comprising:

generating a first reference current;

generating a second reference current;

simultaneously comparing a bit line current from a column coupled to the non-volatile memory cell with the first reference current and the second reference current;

identifying if the memory cell is over-erased, under-erased or erased; and

correcting the memory cell if it is over-erased or under-erased.

34. A method of erase verifying a non-volatile memory cell comprising:

generating a first reference voltage;

generating a second reference voltage;

simultaneously comparing a bit line voltage from a column coupled to the non-volatile memory cell with the first reference voltage and the second reference voltage;

identifying if the memory cell is over-erased, under erased of erased; and

correcting the memory cell if it is over-erased or under-erased.

35. A memory device bit line erase verify circuit comprising:

a first comparator to compare a memory cell current with a first upper reference current and produce a first output signal;

a second comparator to compare the memory cell current with a second lower reference current and produce a second output signal; and

control circuitry coupled to receive the first and second output signals and determine if the memory cell current is within a window defined by the first upper and second lower reference currents.

36. The memory device bit line verify circuit of claim 37 wherein the control circuitry determines that the memory cell is erased if the memory cell current is within the window, the memory cell is over-erased if the memory cell current is greater than the first upper current, and the memory cell is under-erased if the memory cell current is lower than the second lower current.

37. A non-volatile memory comprising:

an array of non-volatile memory cells arranged in columns using bit lines;

a verify circuit selectively coupled to the bit lines to determine if the memory cells have a program level that is within a erase level window defined by first upper and second lower reference signals; and

control circuitry coupled to the verify circuit to determine that the memory cell is erased if the memory cell has a erase level within the window, if the memory cell is over-erased if the memory cell has a erase level greater than the first upper reference signal, and if the memory cell is under-erased if the memory cell has a program level lower than the second lower reference signal.

38. The non-volatile memory of claim 37 wherein the first upper and second lower reference signals are first upper and second lower reference current signals.

39. The non-volatile memory of claim 37 wherein the first upper and second lower reference signals are first upper and second lower reference voltage signals.

40. A non-volatile memory comprising:

an array of non-volatile memory cells arranged in columns using bit lines; and

a verify circuit selectively coupled to the bit lines to simultaneously determine if the memory cells have a erase level that is within a erase level window defined by first and second reference signals.

41. A method of erasing a flash memory device comprising:

pre-programming flash memory cells;

applying erase pulses to the flash memory cells and performing an erase verification of the flash memory cells; and

healing over-erased ones of the flash memory cells without performing a separate leakage detection operation.

42. The method of claim 41 wherein over-erased flash memory cell addresses are latched during the erase verification of the flash memory cells.

43. The method of claim 41 wherein healing over-erased flash memory cells is embedded within performing the erase verification of the flash memory cells.

44. A method of erasing a flash memory device comprising:

pre-programming flash memory cells;

applying erase pulses to the flash memory cells and performing an erase verification of the flash memory cells; and

healing over-erased ones of the flash memory cells is embedded within performing the erase verification of the flash memory cells.